

FIG. 1

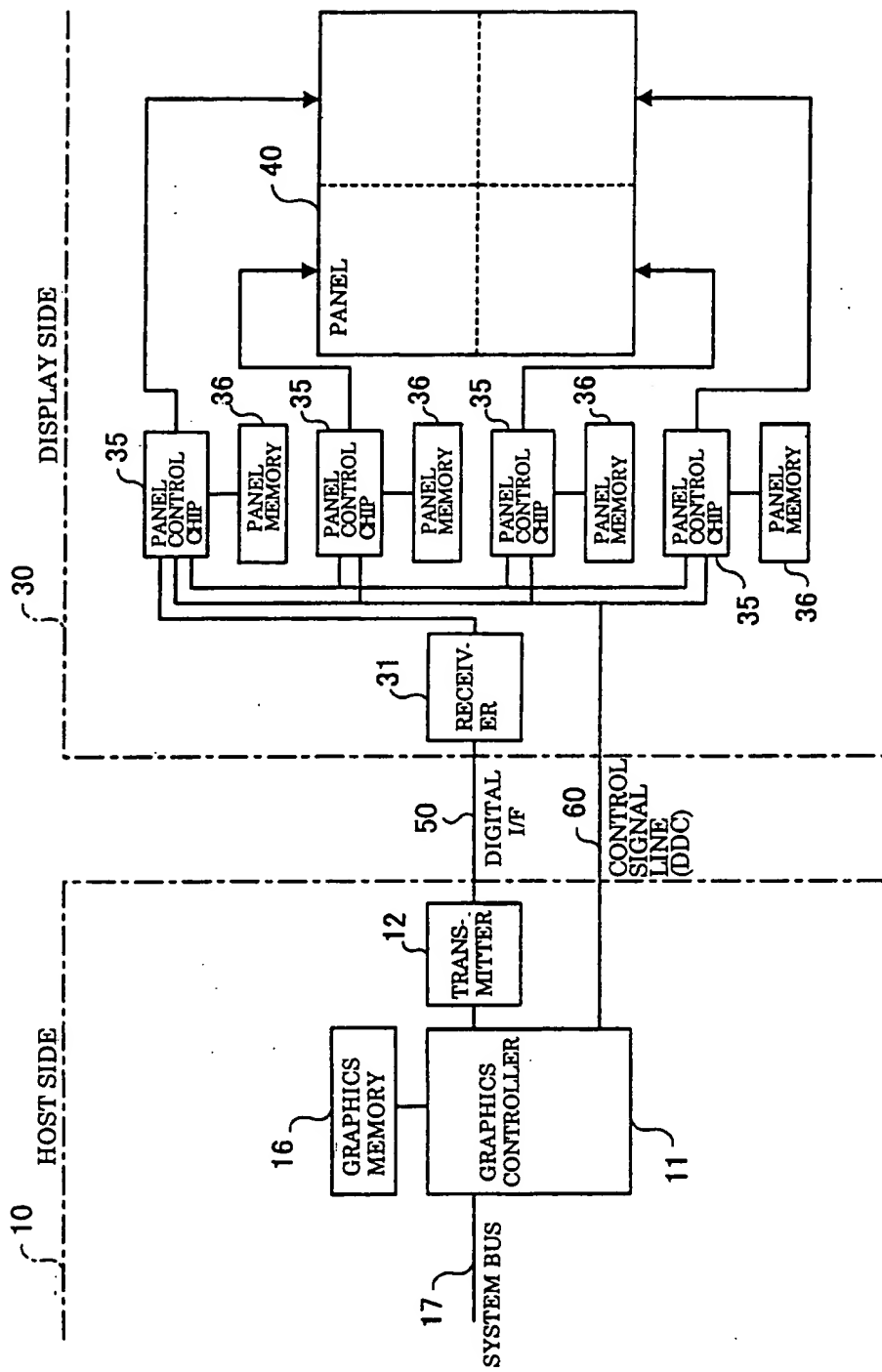
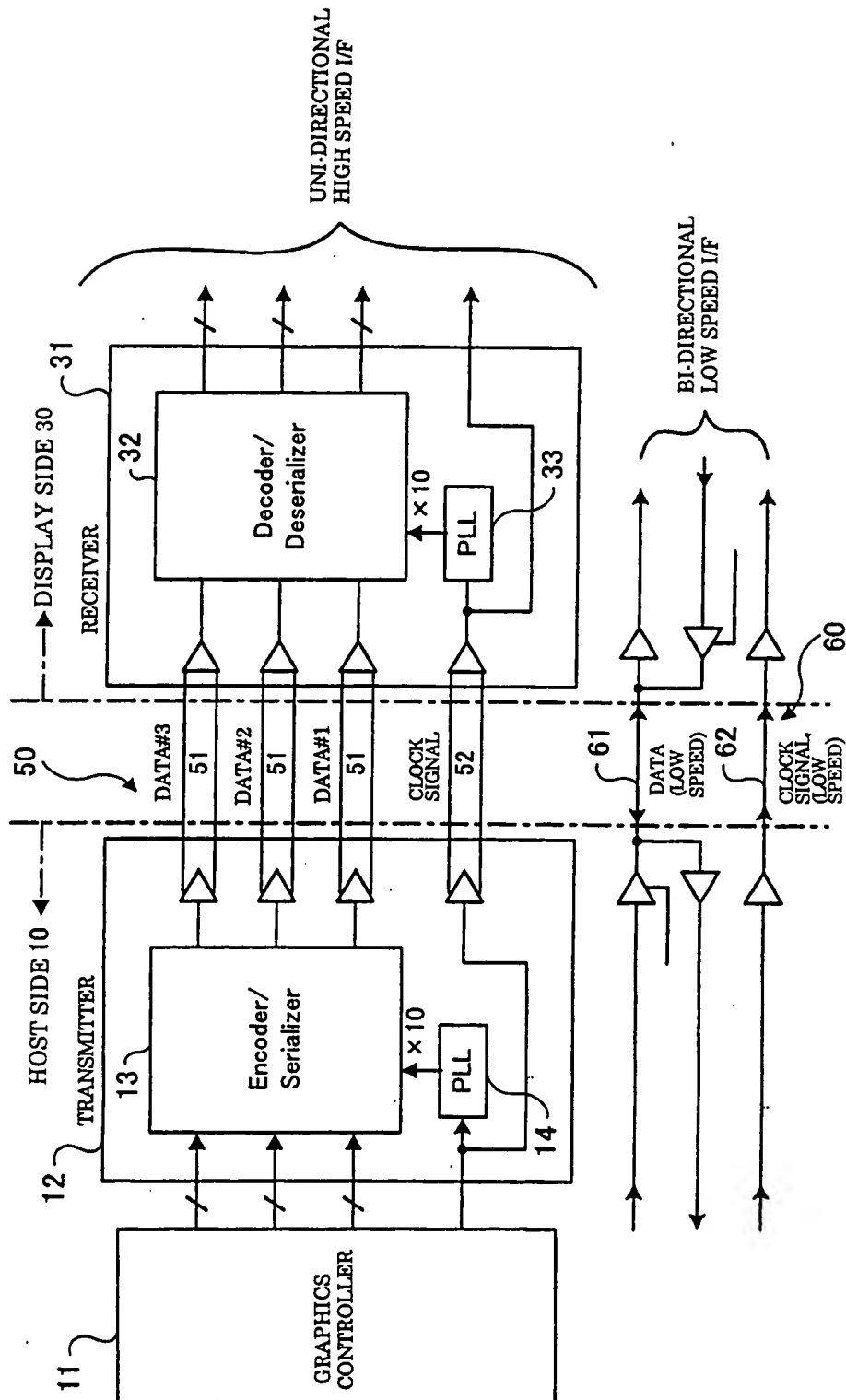


FIG. 2



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FIG. 3

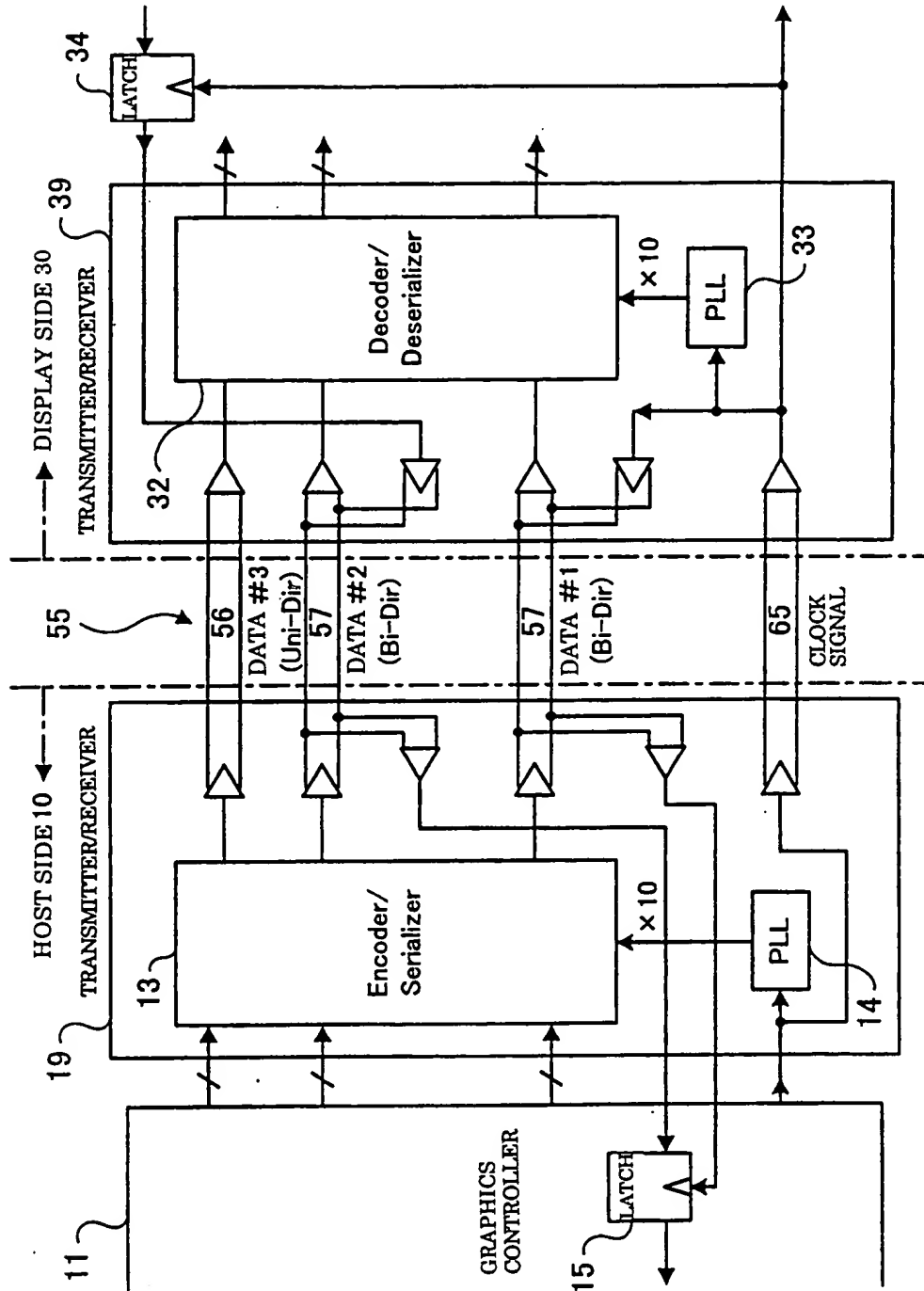


FIG. 4

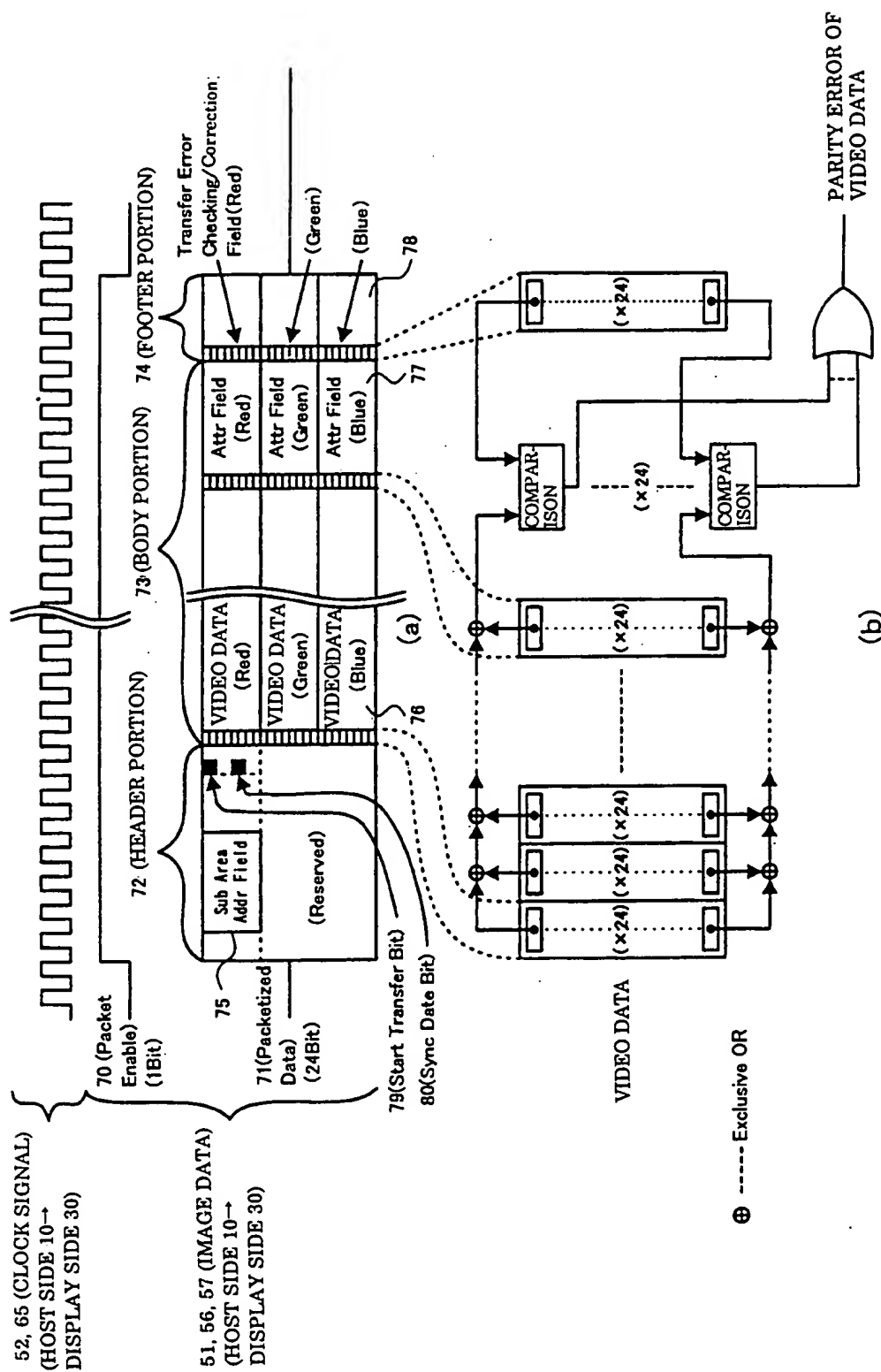
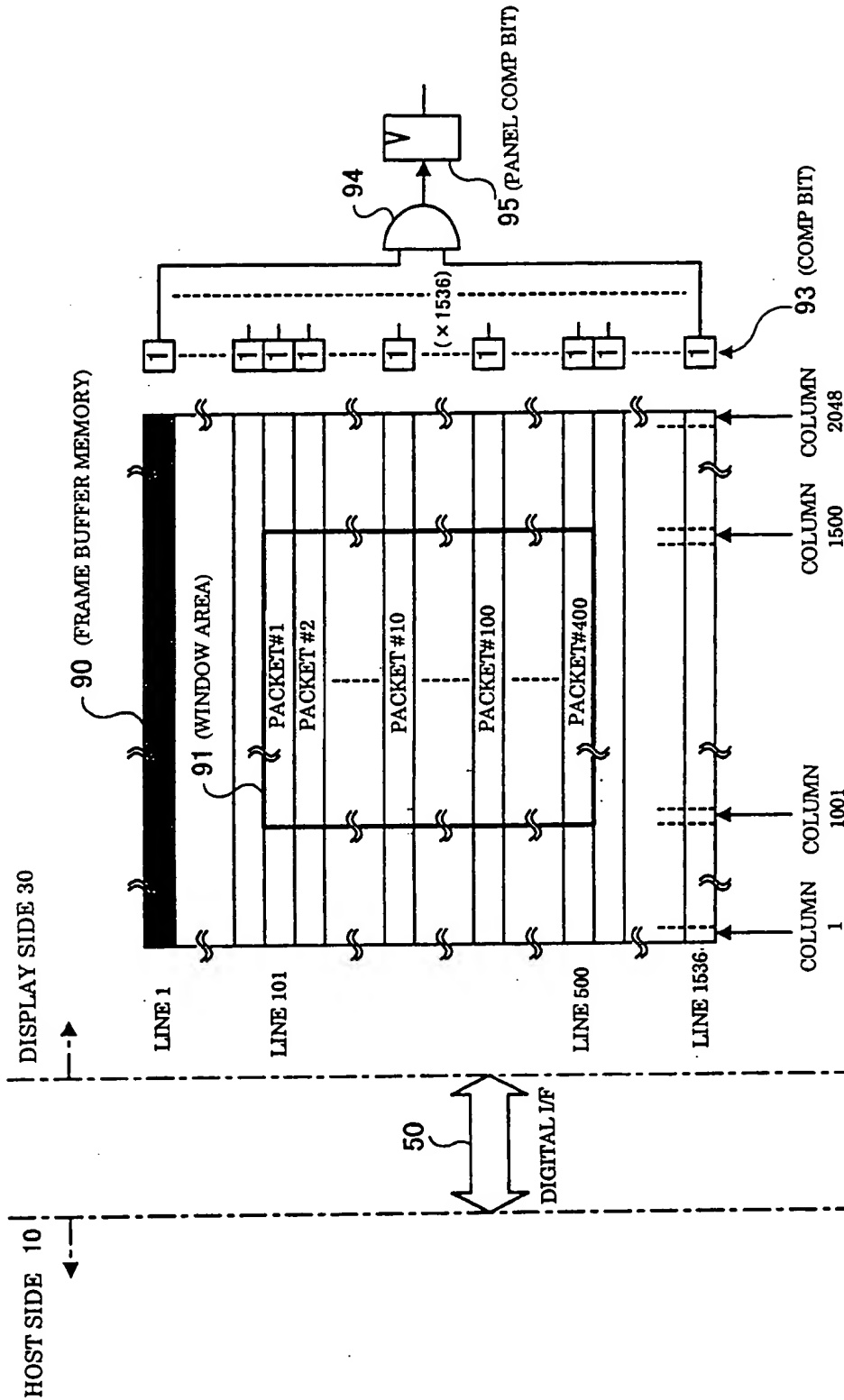


FIG. 5



[illegible]

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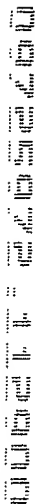
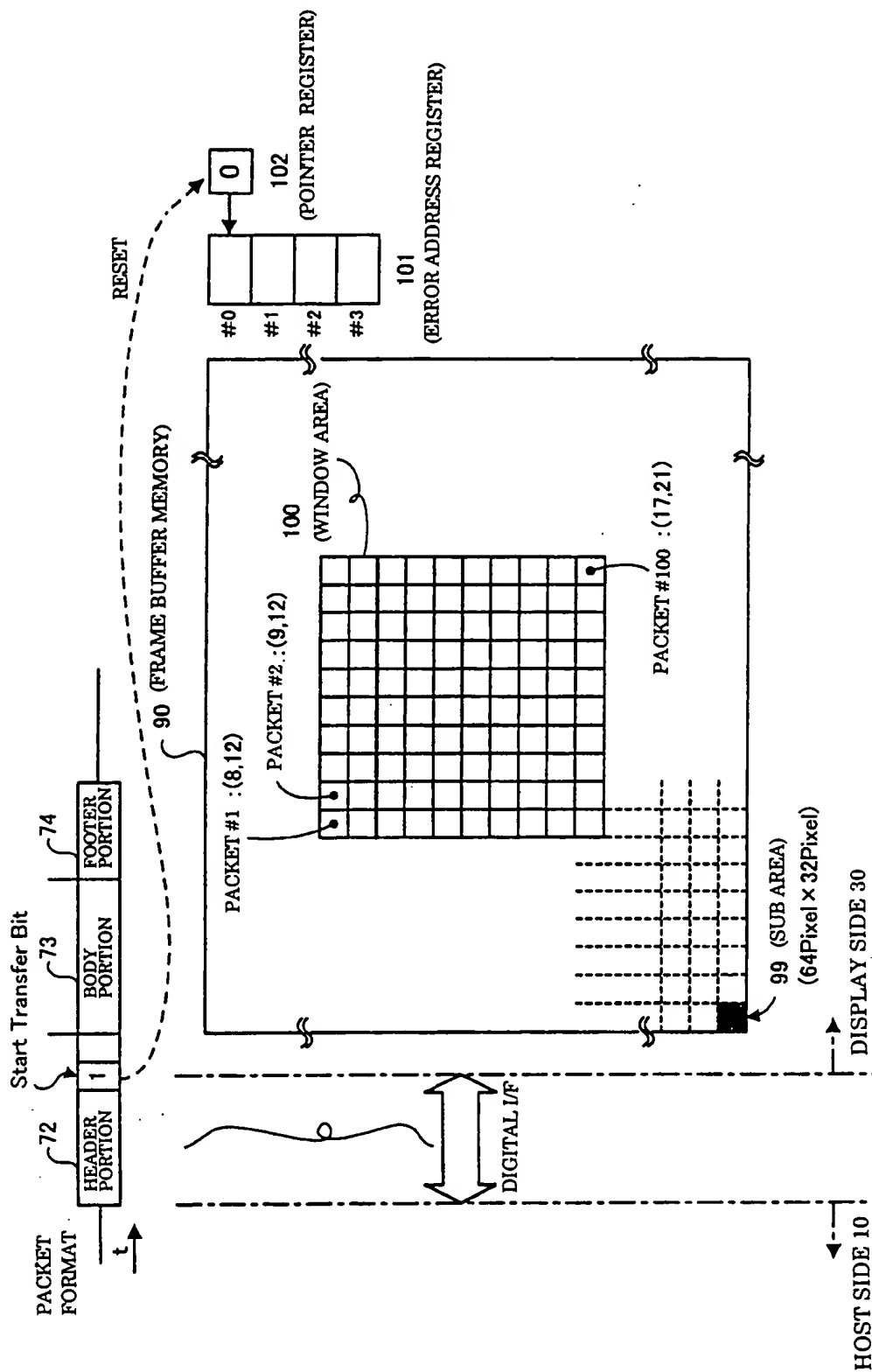


Figure 1 is a block diagram of a video display system. The system is divided into a HOST SIDE 10 and a DISPLAY SIDE 30, connected by a DIGITAL I/F 12. On the HOST SIDE 10, a packet 93 (COMP BIT) is shown as a sequence of bits 1. This packet is sent to the DISPLAY SIDE 30 via the DIGITAL I/F 12. On the DISPLAY SIDE 30, the packet 93 is compared with a reference 94 (PANEL COMP BIT) using a comparator 95. The result of the comparison is sent to a control unit 96, which then outputs a signal 97 to a frame buffer memory 90. The frame buffer memory 90 outputs data to a window area 91, which is displayed on the display side 30. The display side 30 shows a grid of lines (1 to 1536) and columns (1 to 2048). A packet 93 is shown as a sequence of bits 1. The diagram also shows a packet 93 (COMP BIT) and a panel comparison bit 95 (PANEL COMP BIT) being used to compare the packet with a reference 94. The result of the comparison is sent to a control unit 96, which then outputs a signal 97 to a frame buffer memory 90. The frame buffer memory 90 outputs data to a window area 91, which is displayed on the display side 30. The display side 30 shows a grid of lines (1 to 1536) and columns (1 to 2048). A packet 93 is shown as a sequence of bits 1.

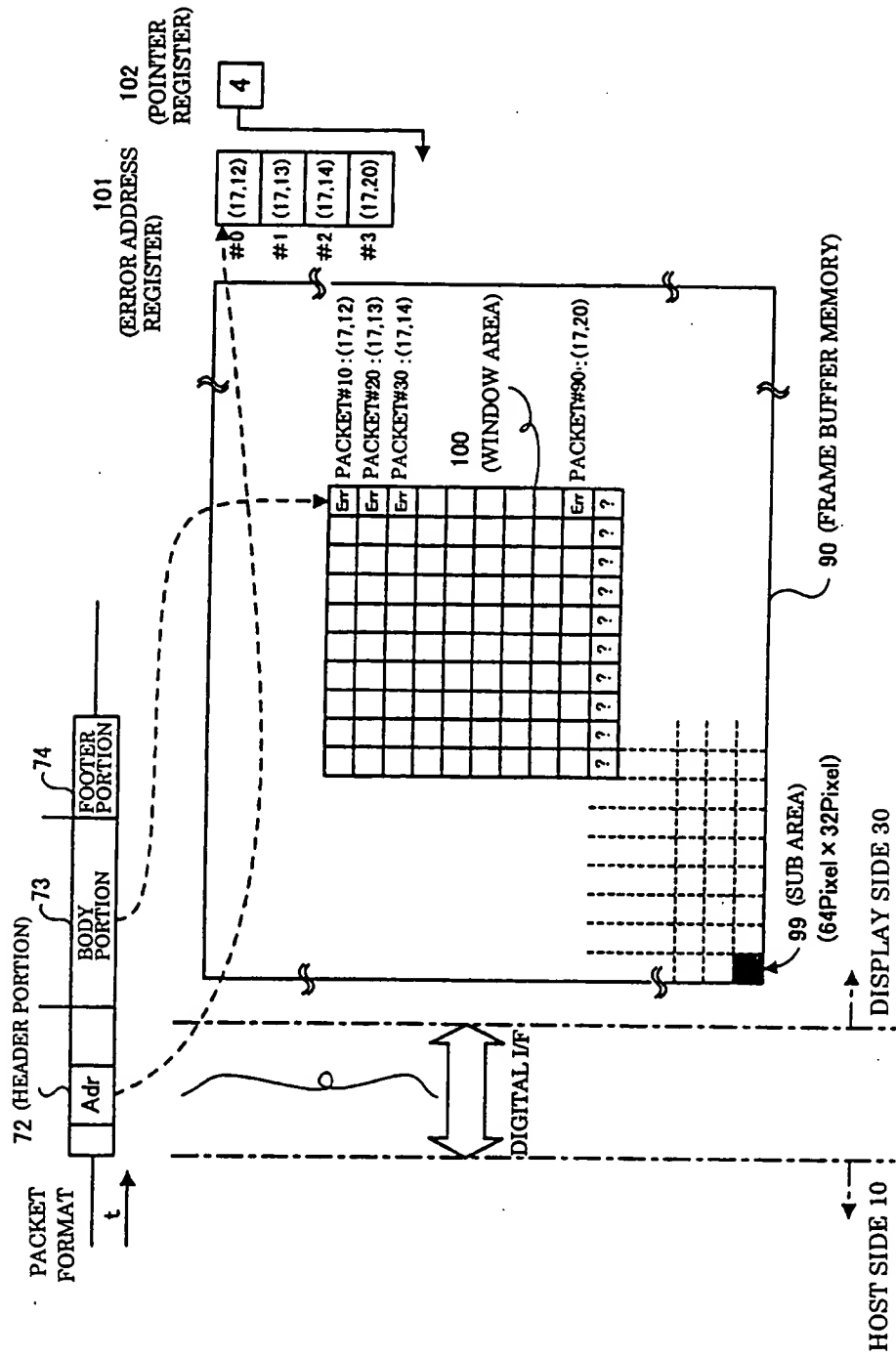
FIG. 8





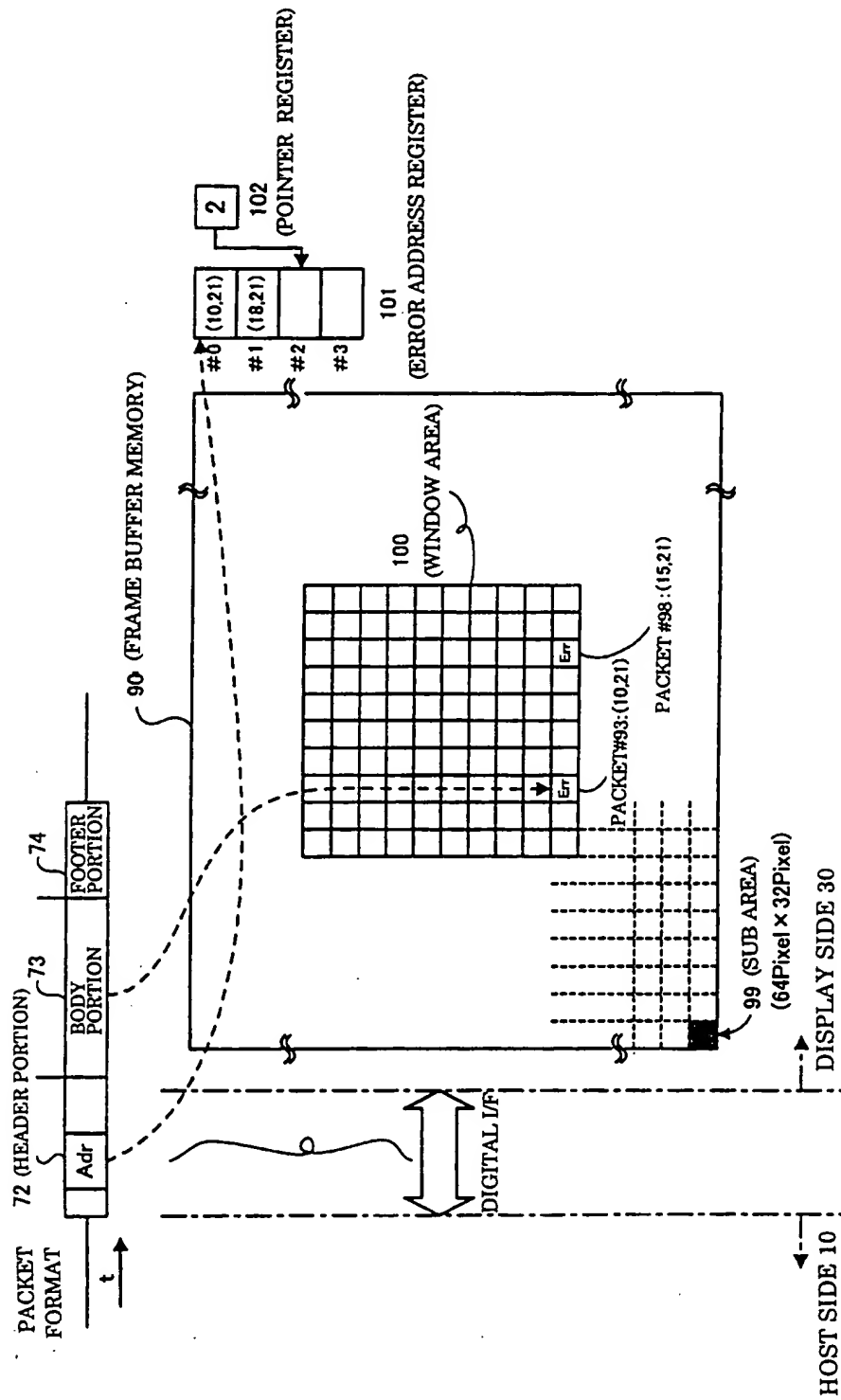
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FIG. 9



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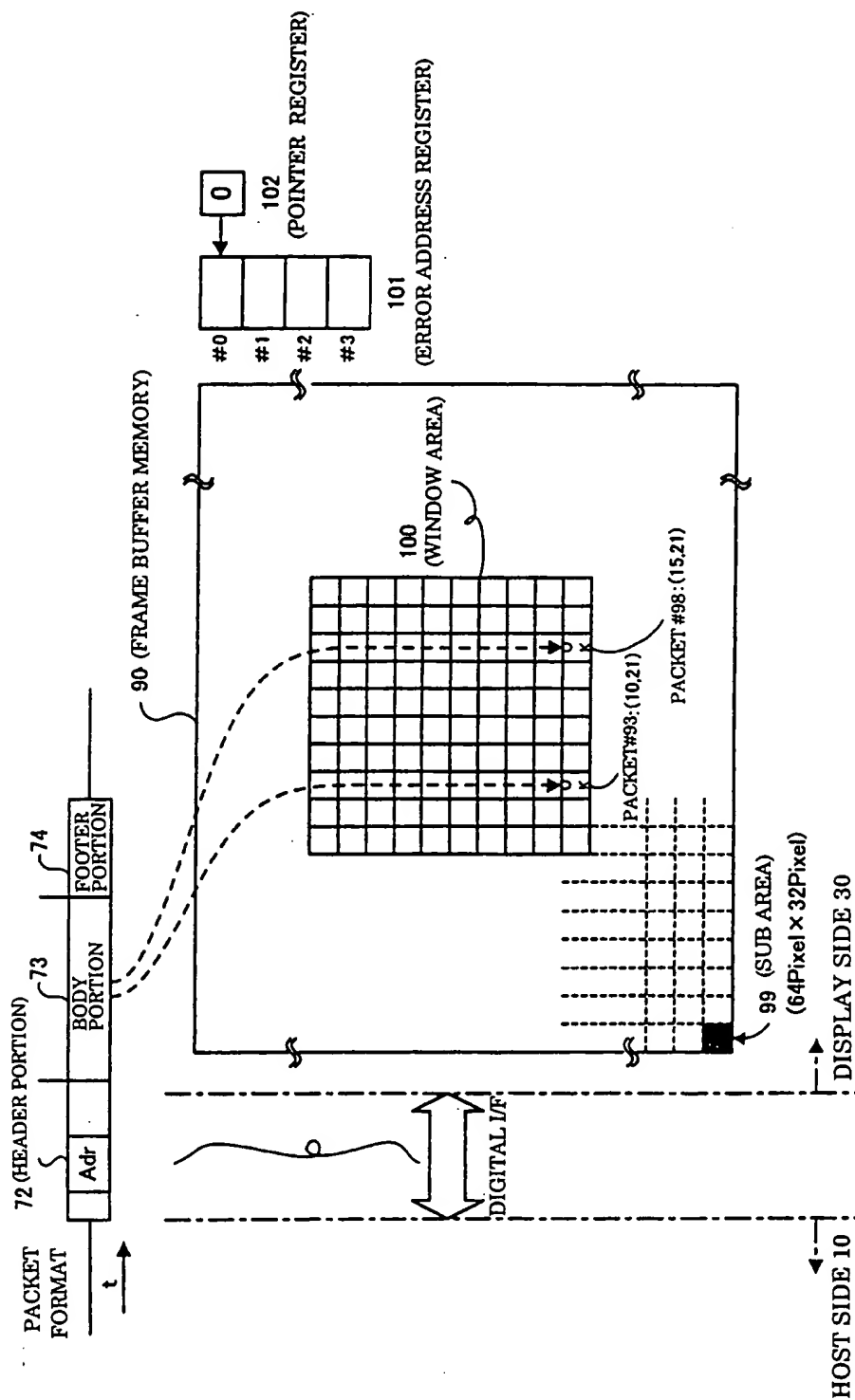
FIG. 10



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FIG. 11



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FIG. 12

